WHAT IS CLAIMED IS:

1. A method for fabricating semiconductor components comprising:

providing a substrate containing the components;

testing the components on the substrate to evaluate and map the components; and

forming a plurality of electrical conductors on the substrate using a laser imaging process and data from the testing step, such that the conductors are configured to repair, re-configure or electrically isolate at least one component.

2. The method of claim 1 wherein the substrate comprises a semiconductor wafer and the components comprise semiconductor dice or semiconductor packages.

3. The method of claim 1 wherein the forming step comprises forming a metal layer on the components, forming a radiant sensitive film on the metal layer, laser imaging the radiant sensitive film to form a mask, and then etching the metal layer through the mask.

4. The method of claim 1 wherein the forming step comprises forming a radiant sensitive film on the substrate, laser imaging the radiant sensitive film to form a mask having a plurality of openings, and then depositing an electrically conductive material through the openings to form the conductors.

5. The method of claim 1 wherein the testing step evaluates various electrical characteristics of the components, and the at least one component comprises a defective component.

6. A method for fabricating semiconductor components comprising:

providing a substrate containing the components;

testing the components on the substrate to identify a defective component;

providing a laser scanner;

forming an electrically conductive layer on the components;

forming a radiant sensitive film on the layer;

exposing the film using laser imaging and data from the testing step to form a mask; and

etching the layer through the mask to form a plurality of conductors configured to repair or to electrically isolate the defective component.

7. The method of claim 6 wherein the components comprises memory devices and the conductors re-configure the defective component in a selected format.

8. The method of claim 6 wherein the conductors substitute redundant circuitry to repair the defective component.

9. The method of claim 6 wherein the components comprise a plurality of component contacts and the conductors interconnect or electrically isolate selected component contacts on the defective component.

10. The method of claim 6 further comprising following the etching step, burn-in testing the components.

11. The method of claim 6 wherein the testing step evaluates various electrical characteristics of the components.

12. The method of claim 6 wherein the testing step maps the components on the substrate.

13. The method of claim 6 wherein the components comprise a plurality of component contacts and the testing step evaluates pad leakage from the component contacts.

14. The method of claim 6 wherein the testing step comprises providing a test circuitry configured to apply test signals, and then electrically connecting the test circuitry to the components using a probe card.

15. The method of claim 6 wherein the substrate comprises a semiconductor wafer and the components comprise semiconductor dice or packages.

16. A method for fabricating semiconductor components on a substrate comprising:

testing the components on the substrate to identify and locate at least one defective component and at least one good component; and

forming a plurality of electrical conductors on the substrate using a laser imaging process and data from the testing step, the conductors configured to electrically connect the good component to a test circuitry and to electrically isolate the defective component from the test circuitry.

17. The method of claim 16 wherein the test circuitry comprises burn-in test circuitry.

18. The method of claim 16 wherein the forming step comprises forming a metal layer on the components, forming a radiant sensitive film on the metal layer, laser imaging the radiant sensitive film to form a mask, and then etching the metal layer through the mask.

19. The method of claim 16 wherein the forming step comprises forming a radiant sensitive film on the substrate, laser imaging the radiant sensitive film to form a mask having a plurality of openings, and then depositing an electrically conductive material through the openings to form the conductors.

20. A method for fabricating semiconductor components on a substrate comprising:

testing the components to identify good components and defective components;

providing a laser scanner;

forming a plurality of electrical conductors on the substrate using the laser scanner and data from the testing step, the conductors configured to provide electrical paths to the good components and to electrically isolate the defective components; and

burn-in testing the good components by applying test signals through the conductors while the defective components remain isolated.

21. The method of claim 20 wherein the forming step comprises depositing a metal layer on the components, depositing a radiant sensitive film on the layer, exposing the film using the laser scanner and the data to form a mask, and then etching the layer through the mask to form the conductors.

22. The method of claim 20 wherein the forming step comprises forming a radiant sensitive film on the substrate, laser imaging the radiant sensitive film to form a mask having a plurality of openings, and then depositing an electrically conductive material through the openings to form the conductors.

23. A method for fabricating semiconductor components comprising:

providing the components on a substrate;

testing the components to evaluate and map the components;

forming an electrically conductive layer on the components;

forming a radiant sensitive film on the layer;

providing a laser scanner configured to laser image the film;

exposing the film using the laser scanner and data from the testing step to form a mask; and

etching the layer through the mask to form a plurality of conductors configured to provide electrical paths to the components on the substrate while electrically isolating at least one component on the substrate.

24. The method of claim 23 further comprising burn-in testing the components while the at least one component remains electrically isolated.

25. The method of claim 23 wherein the substrate comprises a semiconductor wafer and the components comprise semiconductor dice or packages.

26. The method of claim 23 wherein the testing step evaluates a gross functionality and electrical characteristics of the components.

27. A method for fabricating semiconductor components comprising:

providing the components on a substrate;

testing the components to evaluate the components and to locate good components and defective components;

forming a radiant sensitive film on the substrate;

providing a laser scanner configured to laser image the film;

exposing the film using the laser scanner and data from the testing step to form a mask comprising a plurality of openings; and

depositing an electrically conductive material in the openings to form a plurality of conductors configured to provide electrical paths to the good components while electrically isolating the defective components.

28. The method of claim 27 wherein the testing step evaluates a gross functionality and electrical characteristics of the components.

29. The method of claim 27 wherein the testing step comprises providing a test circuitry configured to apply test signals, and then electrically connecting the test circuitry to the components using a probe card.

30. A method for fabricating semiconductor components on a substrate comprising:

testing the components on the substrate to identify good components and at least one defective component; and

forming a plurality of electrical conductors on the substrate using a laser imaging process and data from the testing step, the conductors configured to electrically connect the good components in one or more clusters that exclude the defective component.

31. The method of claim 30 wherein the substrate comprises a semiconductor wafer and the components comprise semiconductor dice or packages.

32. The method of claim 30 wherein the forming step comprises forming a metal layer on the components, forming a radiant sensitive film on the metal layer, direct imaging the radiant sensitive film using to form a mask, and then etching the metal layer through the mask.

33. The method of claim 30 wherein the forming step comprises forming a radiant sensitive film on the substrate, laser imaging the radiant sensitive film to form a mask having a plurality of openings, and then depositing an electrically conductive material through the openings to form the conductors.

34. A method for fabricating semiconductor components on a substrate comprising:

testing the components on the substrate to identify a defective component;

forming an electrically conductive layer on the components;

forming a radiant sensitive film on the layer;

providing a laser scanner configured to laser image the film;

exposing the film using the laser scanner and data from the testing step;

developing the film to form a mask; and

etching the layer through the mask to form a plurality of conductors on the substrate, with at least some of the conductors configured to electrically connect selected components in one or more clusters that exclude the defective component.

35. The method of claim 34 wherein the substrate comprises a semiconductor wafer and the components comprise semiconductor dice or packages.

36. The method of claim 34 wherein the testing step evaluates electrical characteristics of the components.

37. A method for fabricating semiconductor components on a substrate comprising:

testing the components on the substrate to identify a defective component;

forming a radiant sensitive film on the substrate;

providing a laser scanner configured to laser image the film;

exposing the film using the laser scanner and data from the testing step;

developing the film to form a mask comprising a plurality of openings; and

depositing an electrically conductive material in the openings to form a plurality of conductors on the substrate, with at least some of the conductors configured to electrically connect selected components in one or more clusters that exclude the defective component.

38. The method of claim 37 wherein the testing step evaluates electrical characteristics of the components.

39. The method of claim 37 wherein the testing step comprises providing a test circuitry configured to apply test signals and electrically connecting the test circuitry to the components using a probe card.

40. A method for fabricating semiconductor components on a substrate comprising:

testing the components on the substrate to identify at least one good component and at least one defective component;

forming a test board using a laser imaging process and data from the testing step, the test board comprising a plurality of test sites configured to electrically engage the good component but not the defective component; and

burn-in testing the good component using the test board.

41. The method of claim 40 wherein the substrate comprises a semiconductor wafer and the components comprise semiconductor dice or packages.

42. The method of claim 40 further comprising forming a plurality of conductors on the components using a laser scanner and the data.

43. A method for fabricating semiconductor components on a substrate comprising:

testing the components to identify good components and at least one defective component;

providing a test board;

forming an electrically conductive layer on the test board;

forming a radiant sensitive film on the layer;

providing a laser scanner configured to laser image the film;

exposing the film using the laser scanner and data from the testing step to form a mask; and

etching the layer through the mask to form a plurality of test sites on the test board configured to provide electrical paths to the good components while electrically isolating the defective component.

44. The method of claim 43 wherein the substrate comprises a semiconductor wafer and the components comprise semiconductor dice or packages.

45. The method of claim 43 wherein the test board is configured to perform a burn-in test on the components.

46. A method for fabricating semiconductor components on a substrate comprising:

testing the components to identify good components and at least one defective component;

providing a test board;

forming a radiant sensitive film on the substrate;

providing a laser scanner configured to laser image the film;

exposing the film using the laser scanner and data from the testing step to form a mask comprising a plurality of openings; and

depositing an electrically conductive material in the openings to form a plurality of test sites on the test board configured to provide electrical paths to the good components while electrically isolating the defective component.

47. The method of claim 46 wherein the substrate comprises a semiconductor wafer and the components comprise semiconductor dice or packages.

48. The method of claim 46 wherein the test board is configured to perform a burn-in test on the components.

49. A method for fabricating a semiconductor component comprising:

providing a plurality of component contacts on a surface of the component;

forming a radiant sensitive film on the surface and on the component contacts;

exposing the film using a laser imaging process to form a plurality of openings aligned with the component contacts; and

forming terminal contacts in the openings and on the component contacts.

50. The method of claim 49 wherein the laser imaging process is performed using a laser scanner.

51. The method of claim 49 wherein the terminal contacts comprise solder balls.

52. A semiconductor component comprising:

a substrate comprising a plurality of semiconductor components and at least one defective component; and

a plurality of conductors on the substrate configured to provide electrical paths to the components while electrically isolating the at least one defective component.

53. The component of claim 52 wherein the substrate comprises a wafer and the components comprise semiconductor dice or packages.

54. The component of claim 52 wherein the conductors comprise a metal redistribution layer.

55. The component of claim 52 wherein the conductors are configured to electrically connect multiple components in a cluster that excludes the at least one defective component.

56. A semiconductor component comprising:

a substrate comprising a plurality of components comprising a plurality of component contacts and a plurality of terminal contacts in electrical communication with the component contacts;

the components including a defective component; and

a metal layer on the components patterned to form a plurality of conductors configured to provide electrical paths between the components contacts and the terminal contacts and to repair the defective component.

57. The component of claim 56 wherein the conductors electrically connect, or electrically isolate, selected component contacts on the defective component.

58. The component of claim 56 wherein the terminal contacts comprise balls in a grid array.

59. The component of claim 56 wherein the substrate comprises a wafer, and the components comprise dice or packages.

60. A semiconductor component comprising:

a semiconductor die comprising a plurality of integrated circuits and a plurality of component contacts in electrical communication with the circuits;

a plurality of conductors on the die in electrical communication with the component contacts; and

a plurality of terminal contacts on the die in electrical communication with the conductors;

at least some of the conductors configured to interconnect or electrically isolate selected component contacts to repair electrical defects on the die.

61. The component of claim 60 wherein the terminal contacts comprise balls in a grid array.

62. The component of claim 60 wherein the conductors comprise a patterned redistribution layer.

63. A test board for testing semiconductor components on a substrate comprising:

a plurality of test sites on the test board configured to electrically engage the components on the substrate;

the test sites comprising a plurality of conductors configured to provide electrical paths to the components and to electrically isolate at least one component on the substrate.

64. The test board of claim 63 wherein the conductors comprise a laser patterned metal layer.

65. The test board of claim 63 wherein the test board is configured to perform a burn-in test.

66. The test board of claim 63 wherein the substrate comprises a wafer, and the components comprise dice or packages.

67. A system for fabricating semiconductor components comprising:

a substrate comprising a plurality of semiconductor components;

a test circuitry configured to test the semiconductor components; and

a laser scanner configured to pattern a metal layer deposited on the components and the substrate using data obtained by the test circuitry.

68. The system of claim 67 wherein the substrate comprises a semiconductor wafer and the components comprise semiconductor dice or packages.

69. The system of claim 67 further comprising a test board configured to electrically engage the components for performing a burn-in test.

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